IN THE CLAIMS - (CLEAN COPY)

Please amend Claims 1-7, 9-13, 15, and 17-18, as follows. Below are clean copies of the amended claims.

1. (Amended) A process for fabricating an integrated circuit, comprising:

producing several metallization levels, which are mutually separated by interlevel insulating layers;

producing intertrack insulating layers each separating tracks of the same metallization level; and

producing at least one capacitor comprising a lower electrode and an upper electrode which are mutually separated by a dielectric layer, wherein the production of the at least one capacitor comprises:

simultaneously producing, in at least part of an intertrack insulating layer associated with a particular metallization level, on the one hand, [of the two electrodes] the lower electrode, the upper electrode, and the dielectric layer of the at least one capacitor and, on the other hand, simultaneously producing a conducting trench which laterally extends the lower electrode of the capacitor, is electrically isolated from the upper electrode and has a transverse dimension smaller than the transverse dimension of the capacitor; and

producing, in the interlevel insulating layer covering the intertrack insulating layer, two conducting pads which come into contact with the upper electrode of the capacitor and with the conducting trench, respectively.

2. (Amended) The process according to Claim 1, wherein the trench comprises only the conducting material forming the lower electrode.

3. (Amended) The process according to Claim 1, wherein the tracks of a particular metallization level are produced simultaneously with the formation of the upper electrode of the capacitor.

4. (Amended) The process according to Claim 1, wherein the production of the capacitor and of the trench comprises:

a) formation of the intertrack insulating layer on an interlevel insulating layer;

b) etching at least part of the intertrack insulating layer so as to form a cavity having a main part laterally extended by the trench;

c) formation of a first conducting layer of a first conducting material on the structure obtained in step b) and formation of a dielectric layer of a dielectric material on the first conducting layer;

d) formation of a second conducting layer of a second conducting material on the dielectric layer so as to fill the main part of the cavity, the dimensions of the trench and the thickness of the first conducting layer and of the dielectric layer being chosen so as to obtain, after step d), a trench comprising at least the first conducting material but not containing the second conducting material; and

e) chemical-mechanical polishing of the multilayer stack formed in steps c) and d) so as to leave, in the main part of the cavity, the capacitor whose lower electrode is formed from a residual part of the first layer coating of internal walls of the cavity and whose upper electrode is formed from a residual part of the second layer, which is separated from the residual part of the first layer by a residual part of the dielectric layer, and to leave, in the trench, another residual part of the first layer coating of at least internal walls of the trench, to the exclusion of any residual part of the second layer.

A1 cont

5. (Amended) The process according to Claim 4, wherein the trench comprises only the conducting material forming the lower electrode.

6. (Amended) The process according to Claim 4, wherein the tracks of a particular metallization level are produced simultaneously with the formation of the upper electrode of the capacitor.

7. (Amended) The process according to Claim 4, wherein the production of the tracks of a particular metallization level comprises:

after step c), etching the dielectric layer of the first conducting layer and of the intertrack insulating layer so as to form at least one auxiliary trench;

the formation of the second conducting layer being carried out in step d) so as to substantially fill the trench; and

the chemical-mechanical polishing being carried out in step e) so as to remove the first conducting layer, the dielectric layer and the second conducting layer from the surface of the intertrack insulating layer.

9. (Amended) The process according to Claim 8, wherein the trench comprises only the conducting material forming the lower electrode.

10. (Amended) The process according to Claim 8, wherein the tracks of a particular metallization level are produced simultaneously with the formation of the upper electrode of the capacitor.

11. (Amended) The process according to Claim 10, wherein the production of the tracks of a particular metallization level comprises:

after step c), etching of the dielectric layer, of the first conducting layer and of the intertrack insulating layer so as to form at least one auxiliary trench;

the deposition of the second conducting layer carried out in step d) so as to fill the trench or trenches; and

the chemical-mechanical polishing carried out in step e) so as to remove the first conducting layer, the dielectric layer and the second conducting layer from the surface of the intertrack insulating layer.

12. (Amended) An integrated circuit comprising several metallization levels, which are mutually separated by interlevel insulating layers, and intertrack insulating layers each separating the tracks of the same metallization level, and at least one capacitor comprising a lower electrode and an upper electrode which are mutually separated by a dielectric layer, wherein the capacitor is located in at least part of an intertrack insulating layer associated with a particular metallization level, in that the lower electrode of the capacitor is laterally extended by a conducting trench, which is electrically isolated from the upper electrode and has a transverse dimension smaller than the transverse dimension of the capacitor, and in that the integrated circuit comprises, in the interlevel insulating layer covering the intertrack insulating layer, two conducting pads which come into contact with the upper electrode of the capacitor and with the conducting trench, respectively.

13. (Amended) The integrated circuit according to Claim 12, wherein the tracks of a particular metallization level are formed from the material as that forming the upper electrode of the capacitor.

15. (Amended) The integrated circuit according to Claim 14, wherein the tracks of a particular metallization level are formed from the material as that forming the upper electrode of the capacitor.

17. (Amended) The integrated circuit according to Claim 16, wherein the tracks of a particular metallization level are formed from the material as that forming the upper electrode of the capacitor.

18. (Amended) An integrated circuit comprising:

a plurality of metallization levels that are mutually separated by interlevel insulating layers, and intertrack insulating layers each separating the tracks of the same metallization level; and

at least one capacitor comprising a lower electrode and an upper electrode, which are mutually separated by a dielectric layer, and wherein the capacitor is located in at least part of an intertrack insulating layer associated with a particular metallization level, in that the lower electrode of the capacitor is laterally extended by a conducting trench, which is electrically isolated from the upper electrode and has a transverse dimension smaller than the transverse dimension of the capacitor, and wherein, in the interlevel insulating layer covering the intertrack insulating layer, two conducting pads come into contact with the upper electrode of the capacitor and with the conducting trench, respectively, and wherein the tracks of the particular metallization level are formed from the material as that forming the upper electrode of the capacitor.